

## Claims

What is claimed is:

- 1           1.     A method for implementing enhanced performance and  
2 reduced leakage current for application specific integrated circuit (ASIC)  
3 designs comprising the steps of:  
4           identifying standard voltage threshold (SVT) circuits in a circuit  
5 library;  
6           for each SVT circuit, replacing each SVT P-channel field effect  
7 transistor (PFET) with a low voltage threshold (LVT) PFET to provide a  
8 hybrid alternate voltage threshold (AVT) circuit; and  
9           saving each said AVT circuit in an alternate circuit library.
- 1           2.     A method for implementing enhanced performance and  
2 reduced leakage current as recited in claim 1 wherein the step of replacing  
3 each SVT PFET with a low voltage threshold (LVT) PFET includes the step  
4 of adding a low voltage threshold (LVT) over each said SVT PFET.
- 1           3.     A method for implementing enhanced performance and  
2 reduced leakage current as recited in claim 2 wherein the step of adding a  
3 low voltage threshold (LVT) over each said SVT PFET includes the step of  
4 adding a single shape defining said low voltage threshold mask over an  
5 Nwell region to convert each said SVT PFETs to said LTV PFET.
- 1           4.     An alternate voltage threshold (AVT) circuit library comprising:  
2 a plurality of hybrid AVT circuits, each said hybrid AVT circuit  
3 including  
4           each P-channel field effect transistor (PFET) having a low voltage  
5 threshold (LVT); and  
6           each N-channel field effect transistor (NFET) having a standard  
7 voltage threshold (SVT).
- 1           5.     An alternate voltage threshold (AVT) circuit library as recited in  
2 claim 4 wherein said hybrid AVT circuits include a corresponding standard  
3 voltage threshold (SVT) having a low voltage threshold (LVT) added over  
4 each said SVT PFET to convert each said SVT PFET to said LVT PFET.

1           6.     An alternate voltage threshold (AVT) circuit library as recited in  
2 claim 4 wherein each said LVT PFET are provided in an Nwell Region  
3 isolated from each said NFET in each said hybrid AVT circuit.

1           7.     A computer program product for implementing enhanced  
2 performance and reduced leakage current for application specific integrated  
3 circuit (ASIC) designs in a computer system, said computer program product  
4 including instructions executed by the computer system to cause the  
5 computer system to perform the steps of:  
6           identifying standard voltage threshold (SVT) circuits in a circuit  
7 library;  
8           for each SVT circuit, replacing each SVT P-channel field effect  
9 transistor (PFET) with a low voltage threshold (LVT) PFET to provide a  
10 hybrid alternate voltage threshold (AVT) circuit; and  
11           saving each said AVT circuit in an alternate circuit library.

1           8.     A computer program product as recited in claim 7 wherein the  
2 step of replacing each SVT PFET with a low voltage threshold (LVT) PFET  
3 includes the step of adding a low voltage threshold (LVT) over each said  
4 SVT PFET.

1           9.     A computer program product as recited in claim 8 wherein the  
2 step of adding a low voltage threshold (LVT) over each said SVT PFET  
3 includes the step of adding a single shape defining said low voltage  
4 threshold mask over an Nwell region to convert each said SVT PFET to said  
5 LTV PFET.